# DESIGN AND SIMULATION OF 12T MEMORY CELL FOR AEROSPACE APPLICATIONS IN NANO SCALE CMOS TECHNOLOGY

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***Abstract—*** As technology develops, semiconductors' sizes and the spaces between them are becoming smaller and smaller. Because of this, SRAM cells used in aerospace applications are more prone to soft-error when the fragile nodes' basic charge drops. In a typical 6T SRAM cell, a single-event upset (SEU) might result in data inversion if a radiation particle strikes a sensitive node. This research suggests a Soft-Error-Aware Read-Stability-Enhanced Low-Power 12T (SARP12T) SRAM cell to mitigate the effects of SEUs. In comparison with other newly launched soft-error-aware SRAM cells including QUCCE12T, QUATRO12T, RHD12T, RHPD12T, and RSP14T, the performance of SARP12T is assessed. The data could still be recovered even if a radiation assault flips the values of the vulnerable nodes in SARP12T. SARP12T can withstand single-event multi-node upsets (SEMNUs) that are started by a storage node pair. The bitline provides easy access to the '0' storing memory nodes in the proposed cell during read operation, and they are quite resilient to disruptions. Regarding energy usage, the most efficient holding technique is SARP12T. In terms of write performance, SARP12T beats rival cells, and its write latency is significantly reduced. The recommended cell very slightly increases read latency and read/write energy to obtain all of these benefits.

Keywords: SRAM, QUCCE12T, SARP12T, and aerospace

## I. Introduction

The strong ionizing effect of radiation near nuclear reactors and in space has the potential to impair or destroy electrical infrastructure. Ionizing radiation has been linked to circuit failures, notably in data storage devices. The scientific community uses the term "single event upset" (SEU) to describe the occurrence of several ionizing effects of radiation at once [1, 2]. On the one hand, the idea that this radiation doesn't have any effect on long-term memory seems conceivable. When many events occur at once, it may cause an electronic equipment to malfunction, a phenomenon known as the "single event multi-upset effect" (SEMU) [22]. Resetting [7] the electrical cycle with software that employs state machines to recognize prior states might reduce radiation risks. Spending a little amount on space-related applications won't alter this fact [4]. Bit flipping in ionizing CMOS [16] memory is the source of a soft mistake [17]. This impact is due to the expansion of pores in the oxide layer. This strategy makes data storage very sluggish to access. When evaluating SRAM memory in the presence of ionizing radiation, it may be helpful to use a write cycle of different time and complexity to better display the findings. Every new generation of technology results in smaller and more powerful integrated circuit machines. The goal of this technique, which makes use of integrated circuits, is to increase output by packing as many components into a given space as feasible. As Moore's law has been roughly followed, the size of transistors, the fundamental building blocks of memory cells, has risen. So, it stands to reason that cell density will gradually reduce with each succeeding generation [1]. Due to the small size of the transistors used in contemporary technology, each individual cell constitutes a nanoscale system; this is how SRAM-compatible metal-oxide-semiconductor (CMOS) memory is created. As a result, SRAM chips are able to function at steadily decreasing voltages. The International Technological Strategy for Semiconductors (ITRS) predicted that this trend would reverse, but the opposite has already occurred. The scaling limitation on the threshold voltage of the transistor kept the leakage current to an acceptable level [2]. These static random access memories (SRAMs) are essential to the operation of many contemporary electronic devices. This need has been met in large part through the allocation of dedicated space. Costs are anticipated to increase as the predicted number of patients exceeds 90% [3. The technicians are trying to fit as many SRAM cells as they can into each part. Because it results in cells that are smaller in size, this procedure is crucial for improving the technology. SRAMs have transistors that are normally as small and as high up in the architecture as is practicable. Additionally, the voltage is maintained low to ease strain on the electrical system. However, the reduced power usage was only partially implementedin practice. With the development of new technologies, SRAM devices have become smaller and use less power; nonetheless, the design still has to overcome two significant obstacles, namely, cell stability and transient event radiation. This study focuses on the latter phenomenon. However, there are also inquiries into SRAM dependability concerns. In terms of regional radiation, SRAMsare crucial. They might be badly damaged by single-event upsets (SEUs), which are triggered bya single particle of energy. These failures are categorized as soft errors (SE) since they do not permanently harm the circuit. When massive particles collide, they release electron-hole pairs (SEUs), which are gathered in a sensitive region and utilized to control the circuit's power supply. A node in an SRAM array may check the status of a cell and change the data stored in it if there is enough noise. There is no truth to these claims at all. One or more SRAM cells might have theirdata corrupted by a passing particle.

## I. PROPOSED METHOD

This novel radiation-hardened-by-design (RHBD) 12T storage facility features an easily implementable layout-topology and also takes into consideration the physical mechanism of upset in soft faults. The validation results show that the proposed 12T cell can provide significant radiation resistance. The predicted 12T cell requires more room, energy, and time to read and write than a 13T cell. The 986.2 mV margin of static noise in the hold is more than what a 13T cell can achieve. The error-correcting capabilities of the recommended 12T cell make it more trustworthy. These days, CMOS technology is ubiquitous in the electronics sector. The aircraft industry is another that benefits greatly from CMOS technology. Memories are the primary data storage mechanism in many aeronautical applications. CMOS technology is used in the production of SRAM cells, a kind of memory. The main problem with long-term memory is single-event disruptions (SEUs), which are brought on by particles of radiation. Rising urbanization is directly responsible for the SEUs. As CMOS process technology has advanced, both the critical charge and supply voltage have decreased. A approach free of these SEUs is needed for use in aircraft systems. Where exactly dothey exist in the very radioactive void between the stars? Methods that are radiation- hardened by design (RHBD) that are resistant to soft errors are currently being researched. The primary contribution of this study is a proposal for a low-profile, high- reliability RHBD memory cell.

"Adiabatic logic" refers to low-power electrical circuits that may be employed in either direction. During the adiabatic phase, there is no change in the total quantity of heat or energy in the system, thus the name. Energy dissipation is greatly improved by decreasing circuit size and increasing circuit fineness, which has been a major motivation for studying adiabatic circuits.

### *A. SCRL NAND*

Understanding the big picture behind this group of genes may require dissecting the SCRL NA ND completeloop shown in Figure 1.

This ND uses trapezoidal clocks (Kin1 and / Kin1) to power the top and bottom tracks,rather than the more conventional Vdd and Gne 1. There has been no change to this section. With the exception of P 1, which is connected to Gnd, and /P 1, which is connected to Vdd, all components are linked to Vdd/2 in the first position, rendering the switch gate superfluous. The transmission gate is turned on once P 1 and P 1 are configured. First steps. Vdd and Gnd are then created from the /first 1 and /first 1 Vdd/2 nodes. At this stage, the NA ND of both a and b go through the same non-adiabatic door calculation. Once the output is being utilized by the subsequent gate, the transmitting gate may be gradually disabled. The input may be adjusted and the next phase initiated once the sum of phases 0 and 1 reaches Vdd/2 again. Since a deviation from Vdd/2 would violate the first criterion, a resistor must be disabled and the rails reset to this value.

P-MOS's function when coupled with B input is unclear. Please review the circumstances behind the disappearance of the transistor. Times of the eleventh day.

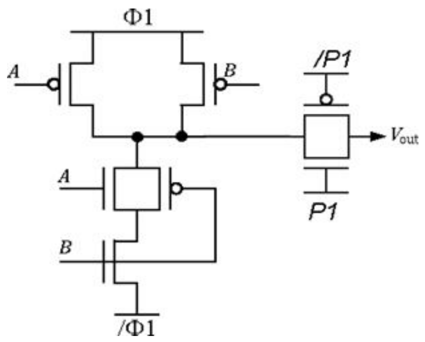



**Figure 1 : SCRL NAND**

### *B. 2LAL*

Frank's[2] Another significant class of adiabatic circuits is the 2LAL family. This series, like SCRL, has complete plumbing all the way to the gate. Figure 2(a) depicts the fundamental components of 2LAL, a pair of transmission gates used to represent the signals A and A. Because of its simplicity and independence from CMOS, 2LAL is well suited for implementation in cutting-edge devices.

Two transmission gates make up the 2LAL basic buffer feature, seen in Figure 2(b). Each trapezoidal clock's zero point on the fourth cycle happens one and a quarter timeslater than the other. Both vertices start out with a value of 0 at the beginning. If the input is 1, the state will change from 0 to 1 over time. When we go on to "phase 1,"

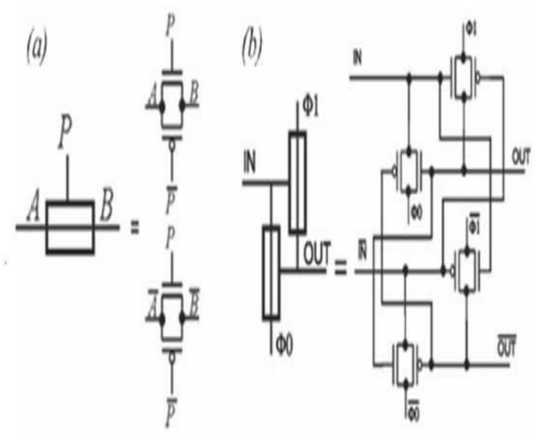
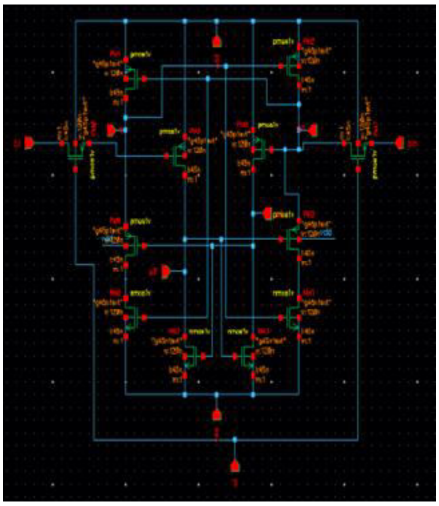



Figure 2: 2LAL Basic Gate(a) and Buffer(b)

When the input is 1, the output and input are both set to 1, and the transistor is disabledto save power. Finally, switch the input back to 0 and keep cycling between 1 and 0. The pipeline is ready to accept a new input after the output passes through the next gate and reverts to 0. 2LAL can build inverters quickly since rails may cross from one portto another.

## II. RESULT

### A. *Proposed schematic*



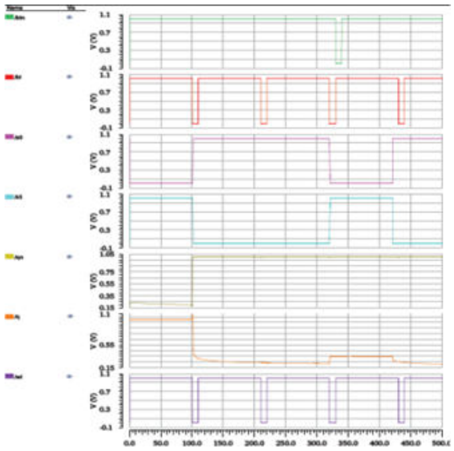


**Figure 3: Proposed schematic**

Figure 4 : proposed schematic simulation result

### A. *DELAY*

```
Parsing                              0.01 seconds
Setup                                0.05 seconds
DC operating point                   0.07 seconds
Transient Analysis                   0.03 seconds
Overhead                             0.91 seconds
-------------------------------------------------
Total                                1.07 seconds
```

### A. *POWER*

```
Power Results

VVoltageSource_3 from time 0 to 100
Average power consumed -> 5.594084e-011 watts
Max power 2.061770e+000 at time 8.025e-008
Min power 8.198842e-003 at time 3.20774e-008
```

## III. CONCLUSION

This novel 12T RHBD memory cell reduces the impact of soft errors in conventional 65 nm CMOS technology. The suggested memory cell is improved upon previous designs in various ways, chief among them being that it is more resilient to disruptions that cause several nodes to be damaged. The process's SEU resilience is further supported by 1000 MC simulations, which show that modifications to the process have no effect on the stability of the SEU. The proposed 12T memory cell's slower read access time in comparison to current memory technologies may cause certain high-speed applications to lag. Mission-critical aviation applications may place a considerably higher value on memory capacity, ruggedness, and dependability. Considering this, in comparison to other cutting-edge hardened memory cells, the RHBD 12T memory cell described in this study is a great design for radiation resistance from the perspective of a crucial application designer. It is typical practice to enhance the paper's speed while reducing its footprint.
The BTI, which alters the transistor's Vth value, is one of the most difficult problems with nano-scale reliability to overcome. SRAM transistors' Vth may be changed, which lowers SNM quality. In this work, we report on a sensor that can accurately identify BTI degradation in SRAM cells, enabling long-term process monitoring. A good indicator of the NBTI/PBTI ageing of individual SRAM cells is the peak Ivdd/Ignd of the SRAM block during a write operation. This current is measured and converted to voltage by the CCVS. The highest value of this voltage establishes the fundamental frequency of the oscillation of the VCO. To see how BTI affects the oscillations, one may compare their frequency to that of freshly formed cells. The BTI state of the row or cell may be seen by reading the relevant item in the SRAM.

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